ABSTRACT OF THE DISCLOSURE

A circuit comprising a register stack and a control circuit. The register stack may be configured as (i) a plurality of segments addressable through a segment address signal and (ii) a plurality of registers within each of the plurality of segments. The plurality of registers are generally addressable through a register address signal. The control circuit may be configured to (i) store a plurality of register states, (ii) store a segment count signal, and (iii) present the segment address signal responsive to the plurality of register states, the segment count signal, and the register address signal.